Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.112”**



**.112”**

**Top Material: Al**

**Backside Material: Au**

**Emitter = .015 x .047”**

**Base = .015 x .030”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .112” X .112” DATE: 10/5/21**

**MFG: MOTOROLA THICKNESS .010” P/N: 2N6193**

**DG 10.1.2**

#### Rev B, 7/1